CLAIMS

What is claimed is:

1. An apparatus, comprising:

a wafer portion that comprises a conduction layer;

wherein upon exposure of the conduction layer during an etch of the wafer portion, the conduction layer serves to dissipate a portion of a charge buildup on the wafer portion.

2. The apparatus of claim 1, wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion;

wherein removal of a portion of the silicon layer from the wafer portion during the etch serves to expose the conduction layer.

3. The apparatus of claim 2, wherein the conduction layer is electrically coupled with the silicon layer of the wafer portion;

wherein the etch serves to create one or more sidewalls in a portion of the silicon layer, wherein the conduction layer is electrically coupled with the one or more sidewalls;

wherein the one or more sidewalls and the conduction layer serve to dissipate the portion of the charge buildup on the wafer portion.

4. The apparatus of claim 3, wherein the one or more sidewalls comprise one or more electrostatic potentials substantially similar to an electrostatic potential of the conduction layer;

wherein the one or more electrostatic potentials of the one or more sidewalls serve to dissipate the portion of the charge buildup from the one or more sidewalls.

5. The apparatus of claim 1, wherein the conduction layer is electrically coupled with a silicon layer of the wafer portion, wherein the wafer portion comprises a backing layer coupled with the conduction layer;

wherein the backing layer provides structural integrity to the wafer portion;

wherein the backing layer insulates the conduction layer.

6. The apparatus of claim 5, wherein the backing layer comprises a photoresist.

7. The apparatus of claim 1, wherein the conduction layer serves to mitigate one or more etch rate variations across the wafer portion.

8. The apparatus of claim 1, wherein the conduction layer neutralizes the portion of the charge buildup on the wafer portion.

9. The apparatus of claim 1, wherein the conduction layer comprises a conductive material.

10. The apparatus of claim 9, wherein the conductive material comprises aluminum.

11. The apparatus of claim 1, wherein the conduction layer comprises a thickness in the range of about one half micrometer ("μm") to about two micrometers.

12. A process, comprising the step of:

dissipating a portion of a charge buildup on a wafer portion through exposure of a conduction layer portion during an etch of the wafer portion.

13. The process of claim 12, wherein the step of dissipating the portion of the charge buildup on the wafer portion through exposure of a conduction layer portion during the etch of the wafer portion comprises the step of:

etching the wafer portion with a Deep Reactive Ion Etch ("DRIE").

14. The process of claim 13, wherein the step of etching the wafer portion with the Deep Reactive Ion Etch comprises the step of:

etching the wafer portion with a Bosch process Deep Reactive Ion Etch.

15. The process of claim 12, wherein the wafer portion comprises a silicon layer and wherein the step of dissipating the portion of the charge buildup on the wafer portion through exposure of a conduction layer portion during the etch of the wafer portion comprises the steps of:

coupling electrically the conduction layer with the silicon layer ;

etching one or more sidewalls in a portion of the silicon layer; and

dissipating, through employment of the one or more sidewalls and the conduction layer, the portion of the charge buildup on the wafer portion .

16. The process of claim 15, wherein the step of coupling electrically the conduction layer with the silicon layer of the wafer portion comprises the step of:

coupling electrically the one or more sidewalls to the conduction layer to keep one or more electrostatic potentials of the one or more sidewalls substantially similar to an electrostatic potential of the conduction layer.

17. The process of claim 12, wherein the step of dissipating the portion of the charge buildup on the wafer portion by the conduction layer exposed during the etch of the wafer portion comprises the step of:

applying the conduction layer to the wafer portion;

etching the wafer portion to a through-etch to expose the conduction layer.

18. The process of claim 17, wherein the step of applying the conduction layer to the wafer portion comprises the step of:

sputtering a conductive material onto the wafer portion to create the conduction layer.

19. The process of claim 18, wherein the conduction layer comprises a first backing layer of the wafer portion, the process, comprising the step of:

applying a backing layer to the conduction layer to protect the conduction layer.

20. The process of claim 12, further comprising the steps of:

etching the wafer portion to a point just before a through-etch;

applying the conduction layer to the wafer portion; and

etching the wafer portion to the through-etch to expose the conduction layer.

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